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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/092,158	06/05/98	MERCHANT S	MERCHANT3333

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2823	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/092,158	Applicant(s) MERCHANT ET AL.	
	Examiner Kurt M. Eaton	Art Unit 2823	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-12 and 14-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-12 and 14-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 2, 5-7, 12, 14, 16, 17, 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. in view of Yamamori.

In re claims 1, 12, and 24, Chung et al. (herein referred to as Chung) shows, in an analogous art related to a wire forming method for a highly integrated device, in Figures 2A-2F, 3A-3B, and 4A-4C depositing a barrier layer (54/56) in a contact opening (h_1) and on at least a portion of a semiconductor substrate (50), thereby exposing a portion of the semiconductor substrate; depositing a contact metal (58) on the barrier layer within the contact opening; and removing a substantial portion of the contact metal and the barrier layer from the semiconductor substrate to form a contact plug within the contact opening, wherein the step of removing the substantial portion of the contact metal and the barrier layer includes etching the contact metal and the barrier layer using a halogen containing etchant {column 3, line 65 - column 6, line 8}.

Chung does not show wherein the barrier layer is deposited by a PVD process nor wherein the contact plug is subject to a temperature sufficient to anneal the barrier layer.

Yamamori shows, in an analogous art related to a method of producing a semiconductor device, in Figures 1A-1D depositing a barrier layer (14/15), wherein the barrier layer is deposited by

a PVD process, in a contact opening (13a) and on at least a portion of a semiconductor substrate (11); depositing a contact metal (16) on the barrier layer within the contact opening; and removing a substantial portion of the contact metal from the semiconductor substrate to form a contact plug within the contact opening, wherein the step of removing the substantial portion of the contact metal and the barrier layer includes etching the contact metal and the barrier layer using a halogen containing etchant. Yamamori further teaches that the halogen component of the halogen containing etchant adheres with an upper surface of the barrier layer to form halogen containing grains of material on the surface of the barrier layer, thereby roughening the surface of the device, thereby preventing material subsequently deposited material to be processed optimally - due to the roughness of the topography. Accordingly, Yamamori teaches subjecting the contact plug to a temperature sufficient to anneal the barrier layer in order to remove the halogen containing grains and allow subsequently deposited materials to be processed optimally, resultant of a smoother device topography {column 1, line 26 - column 4, line 37}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit the barrier layer Chung using a PVD process as disclosed in Yamamori since Chung is silent as to the method by which the barrier layer is formed and the deposition method of Yamamori would enable practitioners of Chung to deposit a barrier layer and the selection of a known barrier layer deposition process on its suitability for the intended use involves only routine skill in the art. It also would have been obvious to subject the contact plug of Chung to a temperature sufficient to anneal the barrier layer as in Yamamori since Yamamori teaches that halogen components in halogen containing etchants capable of etching contact plug material adhere to upper surfaces of barrier layers forming halogen containing grains and thereby inhibiting subsequently deposited materials from being deposited on a smooth surface and being processed

optimally. Subjecting the contact plug of Chung to a temperature sufficient to anneal the barrier layer as in Yamamori would remove the halogen containing grains and allow subsequently deposited materials to be processed optimally.

In re claims 2 and 14, Chung shows wherein depositing the barrier layer includes depositing a titanium layer (54) and depositing a titanium nitride layer (56) on the titanium layer {see Figure 2C; column 4, lines 25-38}.

In re claims 5 and 16, Chung shows wherein depositing the contact metal includes depositing tungsten {column 4, lines 39-44}.

In re claims 6 and 17, Chung shows wherein depositing the contact metal includes depositing tungsten by CVD {column 4, lines 39-49}.

In re claim 7, Yamamori shows wherein subjecting the contact plug to a temperature sufficient to anneal the barrier layer is accomplished using a RTA process {column 4, lines 19-38}.

In re claim 12, Chung in view of Yamamori substantially discloses the invention as claimed but fails to show wherein an active device is formed on the semiconductor substrate, which is in electrical contact with the contact opening.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that an active device would have been formed on the semiconductor substrate of Chung in view of Yamamori such that the contact opening of Chung in view of Yamamori was in electrical contact with the active device since it is well known within the art that active devices are exposed within contact openings so they may be electrically connected with the electrically conductive material formed within the contact openings in order to enable the function of that active device to be realized.

In re claim 18, Yamamori shows wherein subjecting the contact plug to a temperature sufficient to anneal the barrier layer is accomplished using a RTA process for a period ranging from about 5 seconds to about 60 seconds at a temperature ranging from about 600 °C to about 750 °C {column 4, lines 19-38}.

In re claim 23, Chung in view of Yamamori substantially discloses the invention as claimed but fails to show wherein the active device includes forming an active device having a design width of about 0.25 microns or less.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the active devices of Chung in view of Yamamori such that they have a design width of about 0.25 microns or less since a semiconductor substrate containing active devices with a design width of about 0.25 microns or less would minimize the dimensions of the overall device and result in a fabrication process utilizing a higher packing fraction and more efficient use of the space on the substrate. Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the particular dimensions are critical.

4. Claims 4, 8-11, 15, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung in view of Yamamori as applied to claims 1 and 12 above, and further in view of applicants admitted prior art.

In re claims 4 and 15, Chung shows wherein the contact opening is formed in a dielectric (52) {see Figure 2A}.

Chung in view of Yamamori fails to show wherein the contact opening formed the dielectric has an aspect ratio ranging from about 3:1 to about 5:1.

Applicants admitted prior art teaches that it is well known that the semiconductor market demands for faster and more powerful integrated circuits have resulted in significant growth in the number of device per unit area (i.e., a higher packing fraction of active devices). Accordingly, this increased packing fraction means that interconnections for circuits are made to a minimization of dimensions. Accordingly, aspect ratios of contacts are now on the order of about 3:1 to as high as about 5:1 {page 1, line 16 - page 2, line 6}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the contact opening of Chung in view of Yamamori so as to have an aspect ratio of between about 3:1 and about 5:1 as in the applicants admitted prior art since, as evidenced by applicants admitted prior art, in order to provide a device that meets the markets stringent demands and a device with a contacts with aspect ratios between about 3:1 and about 5:1 have the capability to accommodate a higher packing fraction.

In re claims 8, 9, 19, and 20, Chung in view of Yamamori substantially discloses the invention as claimed but fails to show wherein the barrier layer has a thickness ranging from about 5 nm to about 20 nm within the contact opening and wherein a field thickness of the barrier layer outside of the contact opening has a thickness of about 75 nm or greater; nor wherein the thickness of the barrier layer within the contact opening is about 5% to about 20% of the field area thickness.

Applicants admitted prior art teaches that barrier layers deposited by PVD methods within contact openings having aspect ratios large enough to keep up with the market trends in dimensional minimization and packing density maximization may be formed such that the barrier layers may have a thickness ranging from about 5 nm to about 20 nm within the contact openings and a thickness of 75 nm or greater in field areas outside the contact openings and that, because of the irregular topography of the surface of the device, the PVD process deposits barrier layers within the contact

opening only 5% to 20% as thick as portions of barrier layers that are deposited in the field areas outside the contact openings {page 4, lines 1-18}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the barrier layer of Chung in view of Yamamori such that the barrier layer had a thickness ranging from about 5 nm to about 20 nm within the contact opening and wherein a field thickness of the barrier layer outside of the contact opening has a thickness of about 75 nm or greater, wherein the thickness of the barrier layer within the contact opening is about 5% to about 20% of the field area thickness because, as evidenced by applicants admitted prior art, a barrier layer with the aforementioned dimensions would provide a for functioning barrier layer within contact openings having aspect ratios large enough to keep up with the market trends in dimensional minimization and packing density maximization and the difference in barrier layer thickness within and outside contact openings is simply the manifestation of applying a PVD process to deposit a barrier layer within a high performance device capable of keeping up with the market trends in dimensional minimization and packing density maximization. Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the particular dimensions are critical.

In re claims 10, and 21, Chung shows wherein removing a substantial portion includes removing the contact metal and the barrier layer from outside the contact opening {see Figure 2D}.

In re claims 11 and 22, Chung shows wherein the removing the contact metal and the barrier layer includes removing the contact metal and the barrier layer by CMP processes {column 4, lines 50-55}.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 2, 4-12, and 14-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

Wael Fahmy

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